FIG. 1

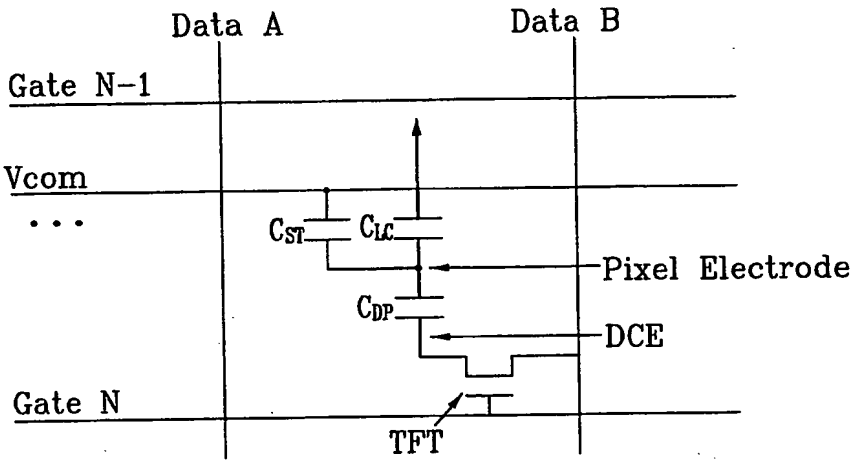
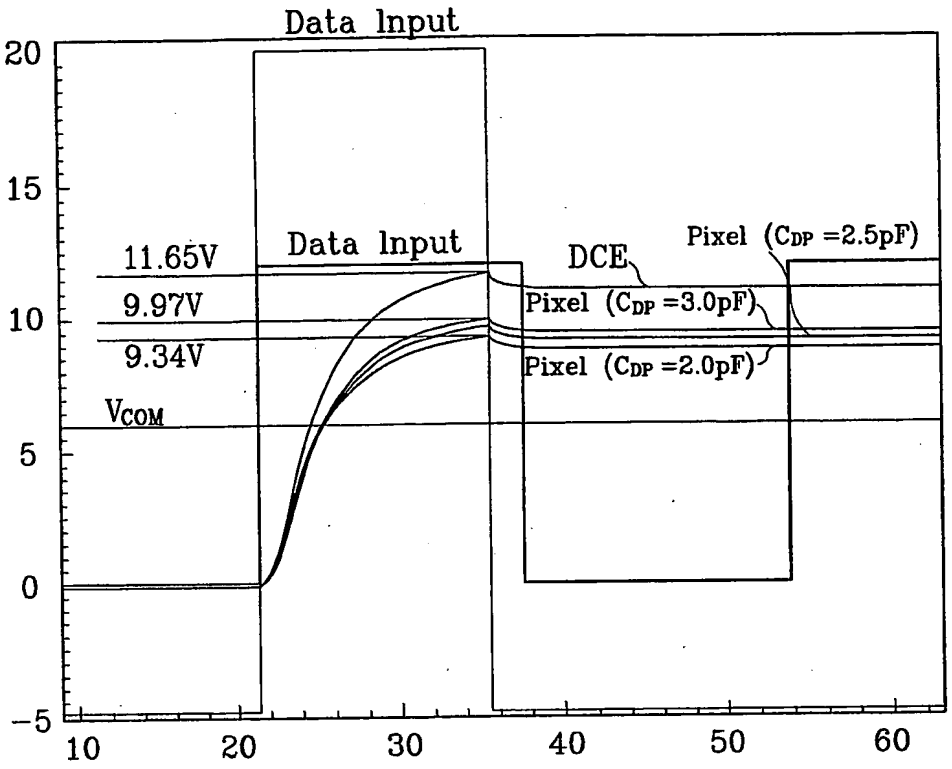

Data A
Data B
Gate N-1
Vcom
• • •
C_{ST}
C_{LC}
Pixel Electrode
C_{DP}
DCE
Gate N
TFT

FIG. 2



Simulation Parameter
TFT W/L=30μm/3.5μm,
C_{DCE_PIXEL}=2.0pF, 2.5pF, 3.0pF (Split)=C_{DP}
C_{DCE_COM}=0.01pF
C_{ST} =0.02pF
C_{LC} =0.3pF
R_{LC} =30T
Gate & Data R,C Load=17" With reference to center

FIG. 3A

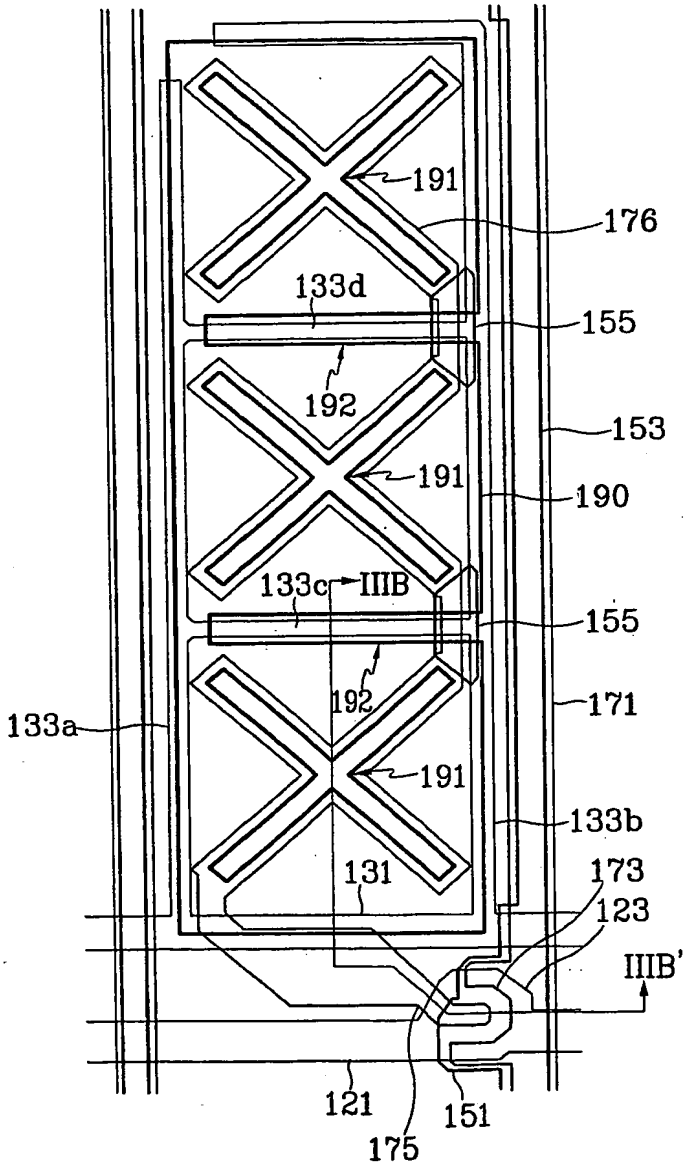

191
176
133d
155
192
153
191
190
133c
IIIB
155
192
171
133a
191
133b
131
173
123
IIIB'
121
151
175

FIG. 3B

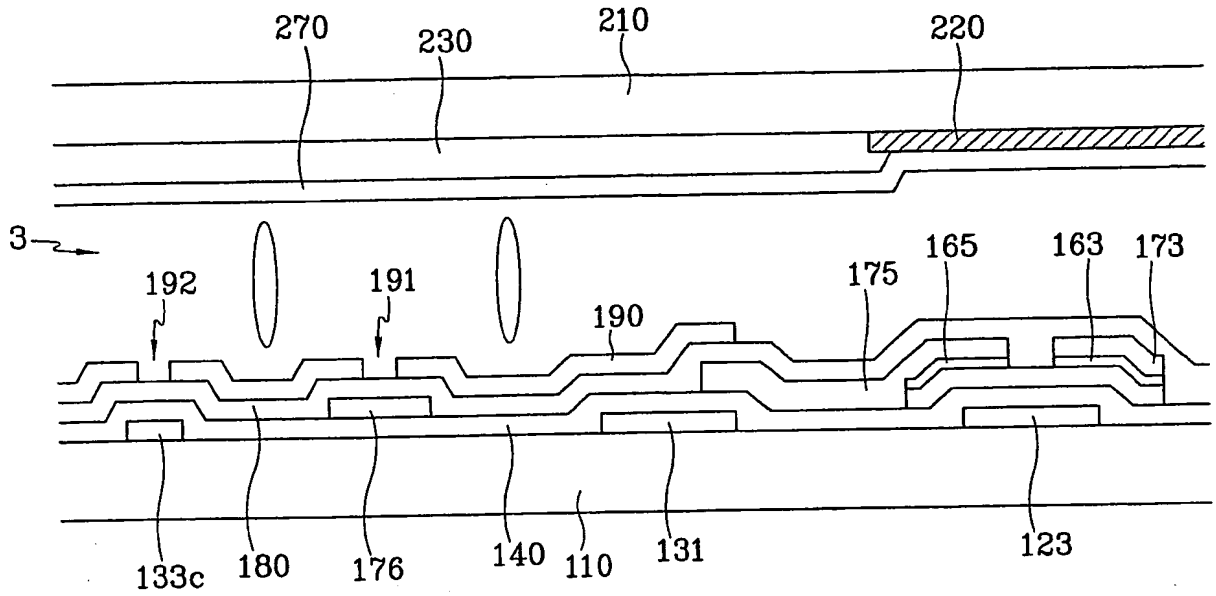

270
230
210
220
3
192
191
190
175
165
163
173
133c
180
176
140
110
131
123

FIG. 4

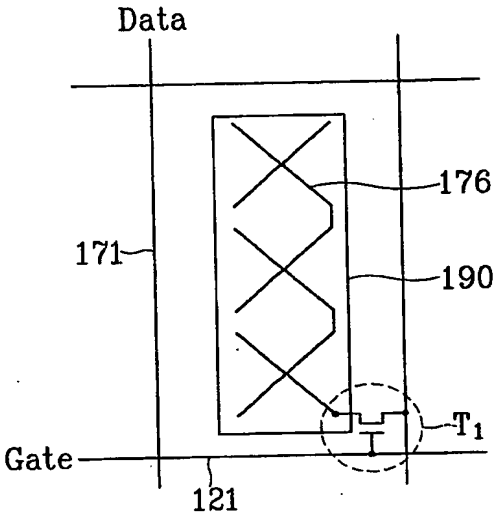


FIG.5

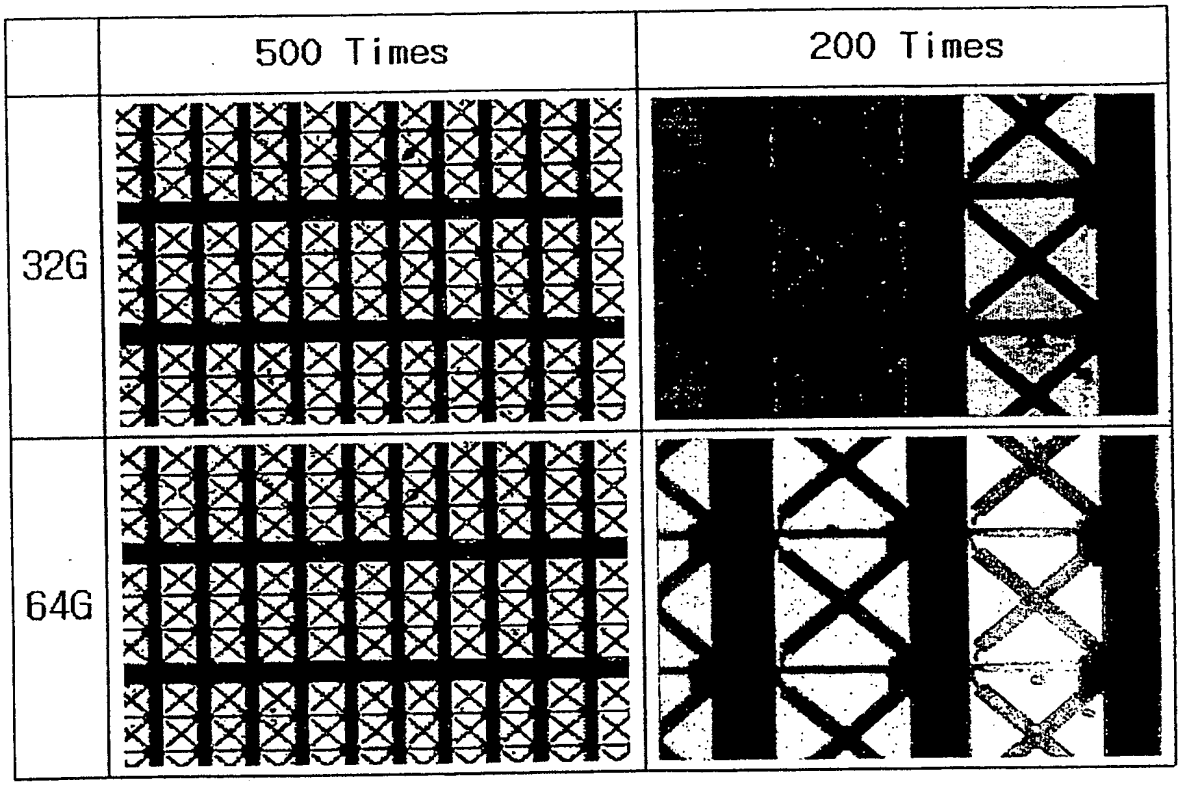


FIG. 6A

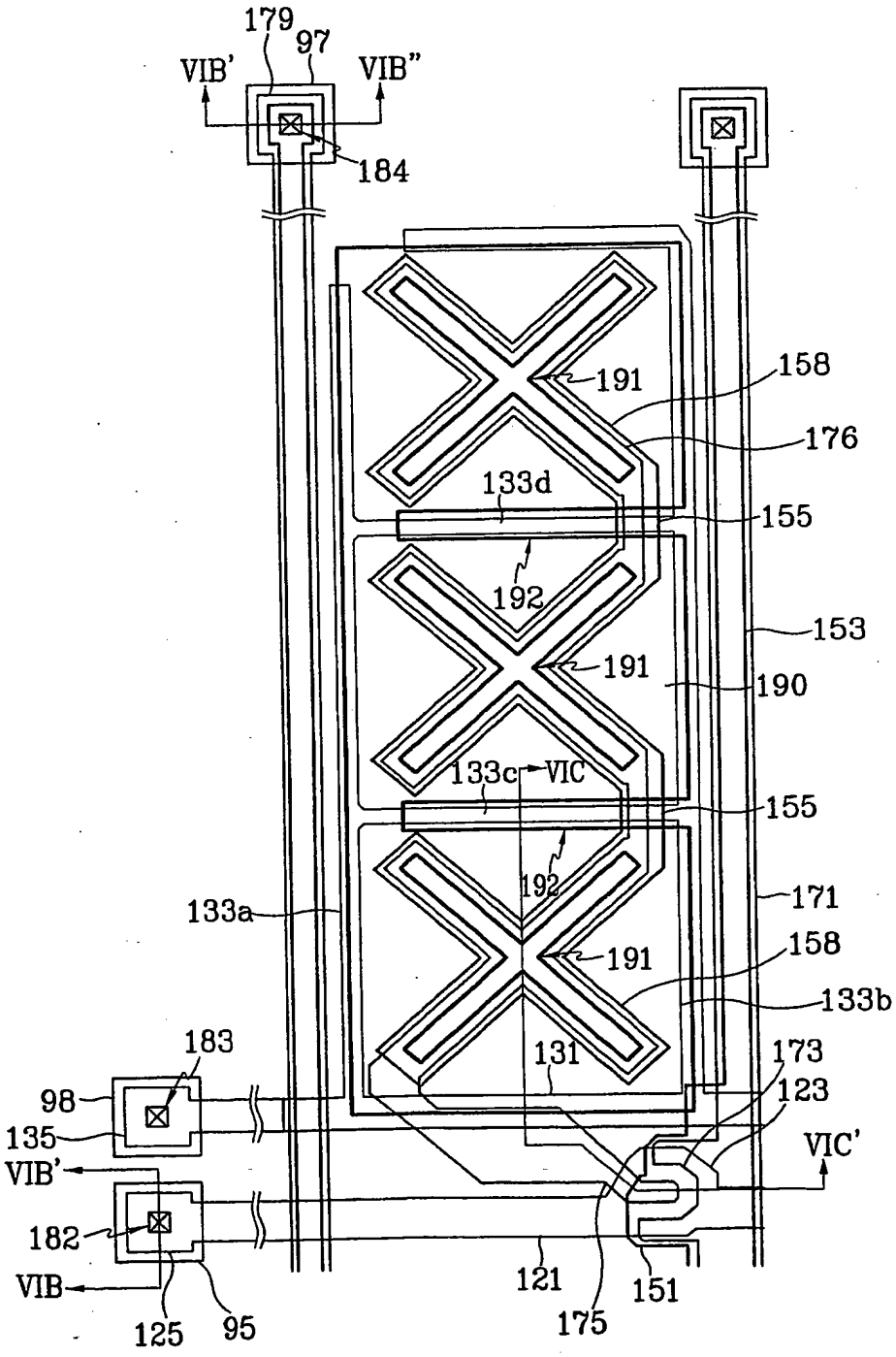

179
97
VIB'
VIB"
184
191
158
176
133d
155
192
153
191
190
133c
VIC
155
192
171
133a
191
158
133b
183
131
173
98
123
135
VIC'
VIB'
182
VIB
121
151
125
95
175

FIG. 6B

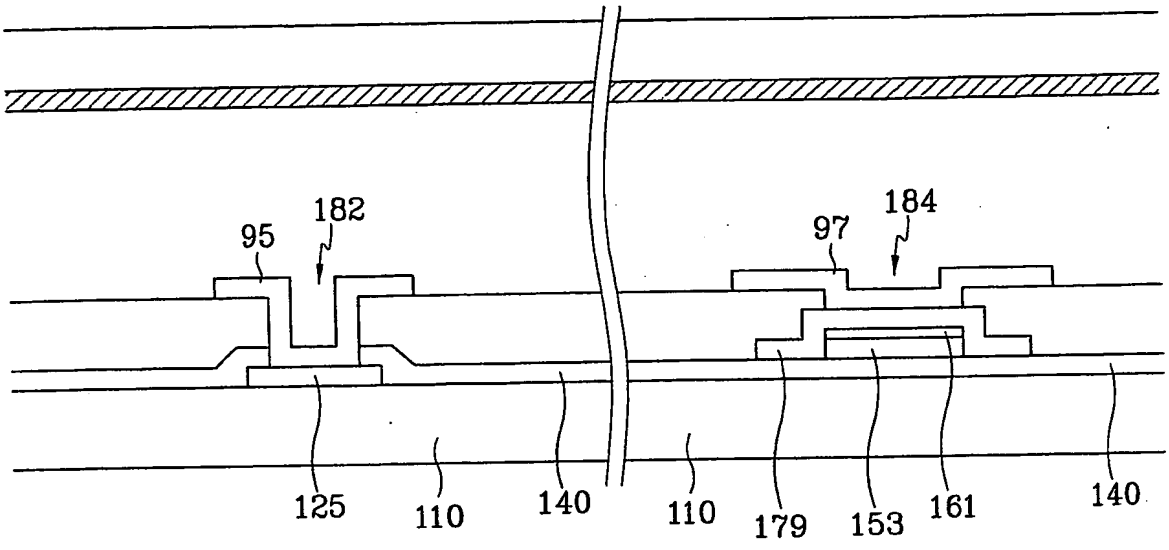

95
182
97
184
125
110
140
110
179
153
161
140

FIG. 6C

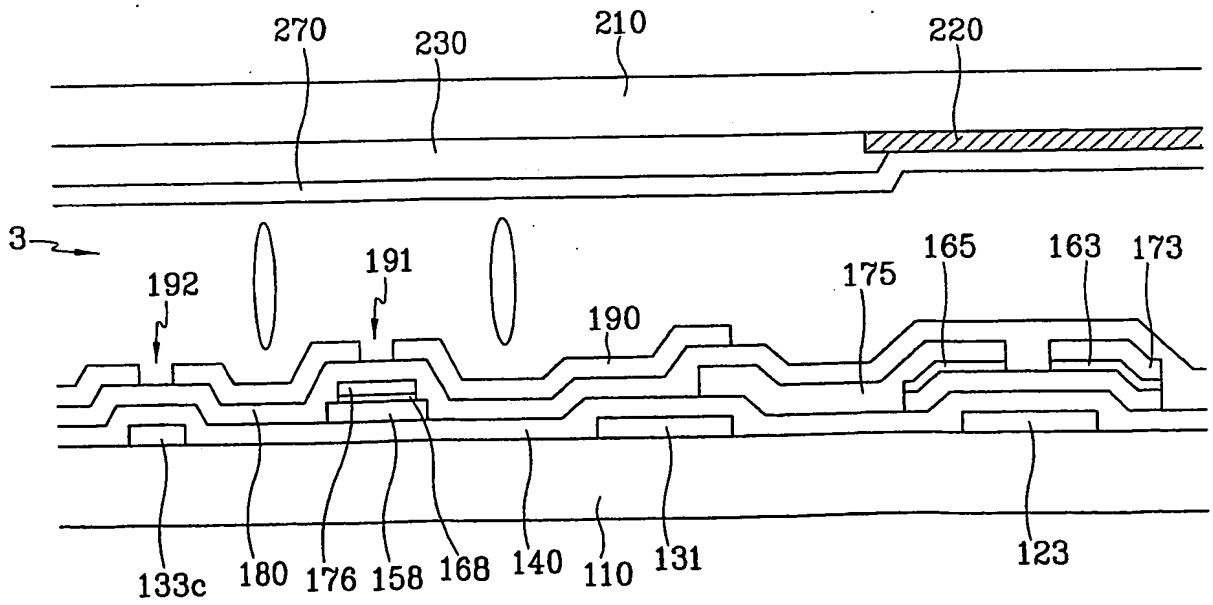

270
230
210
220
3
192
191
190
175
165
163
173
133c
180
176
158
168
140
110
131
123

FIG. 7A

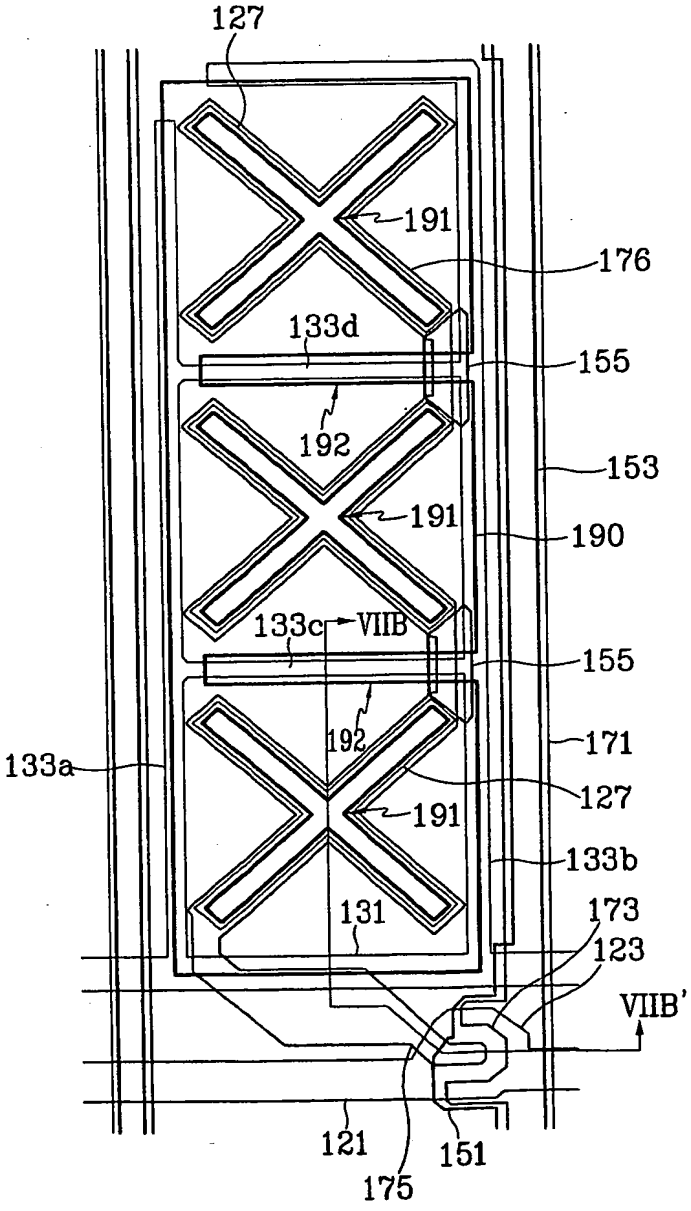
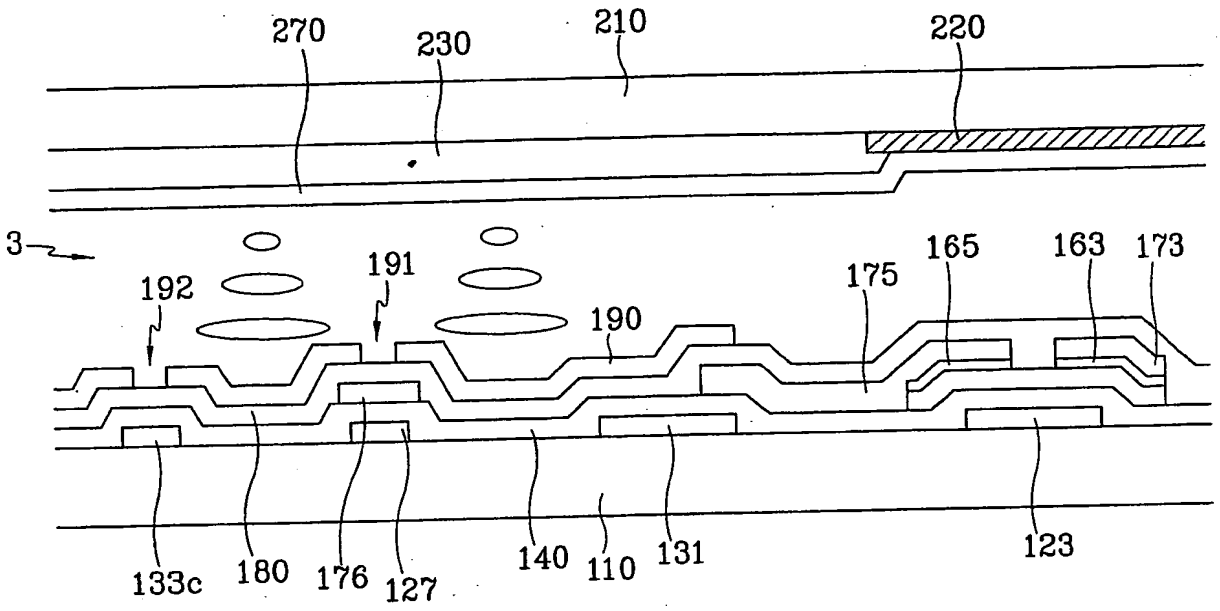

127
191
176
133d
155
192
153
191
190
133c
VIIB
155
192
171
133a
127
191
133b
131
173
123
VIIB'
121
151
175

FIG. 7B


270
230
210
220
3
192
191
190
175
165
163
173
133c
180
176
127
140
110
131
123